REMARKS

Claims 34-40 and 53 have been amended. No new matter has been included. Claims 34-44 and 53-56 remain pending in this application. Applicants reserve the right to pursue the original claims and other claims in this application and in other applications.

Claims 34-44 and 53-56 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The Office Action states that the term "hardwired" in claims 34 and 53 is indefinite. According to the Office Action, hardwired is "used by the claim to mean something that is not programmed and not factory set" whereby according to the Office Action, the "accepted meaning" is "built into a system using hardware such as logic circuits, rather than accomplished through programming." The Office Action further states that "Applicants' specification states that 'the act of hardwiring can be accomplished using a mask programmable photolithographic pattern,'" which the Office Action interprets as "some sort of programming." Office Action p. 2. Applicants respectfully traverse these arguments and the rejection.

Initially, Applicants note that the specification and claims of the present invention do not attempt to redefine the term "hardwired." The specification provides numerous examples of what the Applicant considers to be "hardwired." For example, presence detect data bits are shown as being hardwired to a specific value by connecting a source region of a circuit device to a ground potential. Specification page 10, line 23 to page 11, line 1; and FIG. 4. Other presence detect data bits are shown as being hardwired to a second specific value by forming an open circuit between a source region of a circuit device and a ground potential. Specification page 11, lines 4-7; and FIG. 4. Applicants respectfully submit that these examples fall within the Office Action's definition of hardwired. That is, a short circuit connection to ground and/or

an open circuit are "built into a system using hardware . . . rather than accomplished through programming."

According to the present application, one technique for creating the short and/or open circuits required to hardwire some of the presence detect data is to use a photolithographic mask pattern during the fabrication of metallization layers, or other conductive layers (including e.g., polysilicon contacts, metal contacts, or active regions) of the memory device. Specification page 13, line 25 to page 14, line 29. The Office Action, however, states that the reference to hardwiring using a "mask programmable photolithographic pattern" on page 5 may be interpreted as "some sort of programming." Office Action p. 2. Applicants respectfully traverse this statement. As is known in the art, mask programmable photolithographic patterns, or a programmable mask pattern, refers to the creation of the mask itself. As explained in an exemplary embodiment of the invention, the results of using the "programmable" mask pattern are the desired hardwired open and short circuits discussed above. Specification page 13, line 25-28.

Moreover, Applicants traverse the Office Action's definition of hardwired to the extent the definition requires "logic gates." As indicated in the present application's specification, hardwiring of the presence detect information can occur by connecting a source/drain region to ground or by opening a circuit between a source/drain region and another electrical circuit. Neither of these hardwiring techniques require the use of a logic gate.

In any event, claims 34 and 53 have been amended to clarify what "hardwired" means in the claims. Applicants respectfully submit that the claims are definite and that the rejection based on the term "hardwired" should be withdrawn.

In addition, claims 35-40 stand rejected for allegedly lacking antecedent basis for "said semiconductor memory device." The Office Action states that it is unclear whether this limitation refers to the previously cited "integrated circuit semiconductor memory device" or something else. Applicants respectfully traverse this rejection. Although only one semiconductor memory device is recited in claims 34-40 and Applicants believe it is proper to refer to "said" semiconductor memory device, Applicants have amended claims 35-40 to address the concerns raised in the Office Action.

Accordingly, Applicants respectfully submit that the rejection should be withdrawn and the claims allowed.

Claims 34-40 and 53-56 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,092,146 to Dell et al. ("Dell"). The rejection is respectfully traversed.

Claim 34 recites a signaling circuit for encoding presence detect data. The signaling circuit comprises "a first signal encoding portion for encoding first presence detect information, said first presence detect information being disposed in a hardwired circuit of an integrated circuit semiconductor memory device during the manufacturing of said integrated circuit semiconductor memory device." According to claim 34, "said first present detect data [has] one of a first value associated with a short circuit within said hardwired circuit and a second value associated with an open circuit within said hardwired circuit." The signaling circuit further comprises "a second signal encoding portion for encoding second presence detect information, said second presence detect information being disposed in a programmable circuit of said semiconductor memory device." According to claim 34,"said programmable circuit [is] programmed subsequent to manufacturing of said semiconductor memory device."

Applicants respectfully submit that the Dell reference does not disclose presence detect data "disposed in a hardwired circuit of an integrated circuit semiconductor memory device during the manufacturing of said integrated circuit semiconductor memory device." Moreover, Applicants respectfully submit that the Dell reference does not disclose "first present detect data having one of a first value associated with a short circuit within said hardwired circuit and a second value associated with an open circuit within said hardwired circuit."

As set forth in Applicants prior Amendments, Dell is directed to a memory adapter for configuring SIMMs in a computer system that normally employs DIMMs. Dell col. 1, l. 66 to col. 2, l. 2. The adapter includes a programmable logic device for interrogating and configuring serial presence detect data. Dell col. 2, ll. 2-15. The programmable logic device configures the serial presence detect data by programming an EEPROM whose purpose is to store the serial presence detect data. Dell at col. 2, ll. 4-5 and 13-15. In fact, the primary purpose of the programmable logic device is to program the EEPROM with the serial presence detect data to allow a computer system to access the SIMMs. Dell col. 5, ll. 8-14. In Dell, the EEPROM may be programmed each time that a power-on-reset occurs. *See* Dell Figure 5.

The Dell EEPROM is programmed according to characteristic tables of the programmable logic device. Dell col. 2, ll. 11-13. Table 1 of Dell details the source for the EEPROM programming. According to Table 1, certain serial presence detect data bytes are "factory set." This phrase does not mean, however, that the information is hardwired into the EEPROM. On the contrary, Dell's Figure 5 discloses that the EEPROM may be repeatedly programmed. The fact that certain bytes or information may be re-programmed without change does not teach that this information has been hardwired into the EEPROM. Therefore, Dell does not disclose the storage of presence detect data "disposed in a hardwired circuit of an integrated circuit semiconductor

memory device during the manufacturing of said integrated circuit semiconductor memory device," let alone any device, as recited in claim 34. Moreover, the Dell reference fails to disclose, teach or suggest "first present detect data having one of a first value associated with a short circuit within said hardwired circuit and a second value associated with an open circuit within said hardwired circuit."

In addition, as Applicants established in the parent application, Dell does not disclose, teach or suggest that its memory adapter is "an integrated circuit semiconductor memory device" as recited in claim 34. This is one more reason why claim 34 is allowable over Dell.

For at least the foregoing reasons, Applicants respectfully submit that claim 34 is allowable over Dell. Claims 35-40 depend from claim 34 and are allowable along with claim 34 for at least the reasons set forth above and on their own merits.

Claim 53 recites a method of operating a memory integrated circuit. The method includes the act of "receiving a first signal at a memory controller from said memory integrated circuit, said first signal encoding first presence detect information hardwired into said memory integrated circuit during manufacturing of said memory integrated circuit." According to claim 53, "said first present detect data has one of a first value associated with a short circuit within said memory integrated circuit and a second value associated with an open circuit within said memory integrated circuit." Applicants respectfully submit that Dell fails to disclose the receipt of a signal encoding first presence detect information hardwired into a memory integrated circuit and having "one of a first value associated with a short circuit within said memory integrated circuit and a second value associated with an open circuit within said memory integrated circuit" as recited in claim 53. As such, claim 53 is allowable over

Dell. Claims 54-56 depend from claim 53 and are allowable along with claim 53 for at least the reasons set forth above and on their own merits.

Applicants respectfully request that the rejection be withdrawn and claims 34-40 and 53-57 be allowed.

Claims 41-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dell. The rejection is respectfully traversed. Claims 41-44 depend from claim34 and are allowable along with claim 34 for at least the reasons set forth above and on their own merits. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 34-44 and 53-56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dell in view of U.S. Patent No. 6,275,259 to Gowda. The rejection is respectfully traversed.

Claim 34 recites, among other things, "a first signal encoding portion for encoding first presence detect information, said first presence detect information being disposed in a hardwired circuit of an integrated circuit semiconductor memory device during the manufacturing of said integrated circuit semiconductor memory device" wherein "said first present detect data [has] one of a first value associated with a short circuit within said hardwired circuit and a second value associated with an open circuit within said hardwired circuit." As set forth above, Dell fails to disclose, teach or suggest these limitations (as well as others mentioned above). Applicants respectfully submit that Gowda, which has been cited as teaching hardwiring circuitry, also fails to disclose, teach or suggest these limitations.

As such, the cited combination fails to disclose, teach or suggest the limitations of claim 34. Claims 35-40 depend from claim 34 and are allowable along

with claim 34 for at least the reasons set forth above and on their own merits. Applicants also respectfully submit that claim 53 is allowable over Dell for at least the reasons set forth above. Claims 54-56 depend from claim 53 and are allowable along with claim 53 for at least the reasons set forth above and on their own merits.

Accordingly, the rejection should be withdrawn and the claims allowed.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Dated: September 1, 2005

Respectfully submitted,

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